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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,467	05/07/2004	Che-Li Lin	12919-US-PA	3466

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
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EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
10/01/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/709,467	LIN, CHE-LI	
	Examiner	Art Unit	
	JEFF PIZIALI	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-11,17 and 18* is/are pending in the application.

4a) Of the above claim(s) *5,9,10,17 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8 and 11* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 May 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on *20 July 2009* has been entered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the figures.

Specification

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

5. *Claim 2* is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim (*i.e., claim 1*).

Applicant is required to cancel the claim, or amend the claim to place the claim in proper dependent form, or rewrite the claim in independent form.

Both claim 2 recites, "***said digital color management data is adjustable***." However, this same limitation appears to already be present in claim 1 (*see the last line*).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. *Claims 1-3, 6-8, and 11* are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Kang et al (US 2002/0063666 A1)*** in view of the instant ***Application's Admitted Prior Art (AAPA)***.

Regarding claim 1, ***Kang*** discloses a color management structure [*Fig. 14*] for a panel display [*Fig. 14: 145*], comprising:

a display array unit [*Fig. 14: Clc*];

a plurality of gate drivers [*Fig. 14: 144*];

a plurality of source drivers [*Fig. 14: 143*],

said plurality of gate drivers and said plurality of source drivers driving said display array unit to display an image [*Fig. 14: video data*]; and

a timing sequence control unit [*Figs. 14 & 15: 142*],

said timing sequence control unit outputting a plurality of signals [*Figs. 14 & 15: Gsp, Dclk, RGB, γ data, clock*] to said plurality of gate drivers and said plurality of source drivers to drive said display array unit,

said timing sequence control unit outputting a clock signal [*Figs. 14 & 15: clock -- see also Fig. 9: I^2C clock, serial clock*] and

a digital color management data [*Figs. 14 & 15: γ data, aka User Selectable Gamma Modes A to D -- see also Fig. 9: I^2C Data*] to said plurality of source drivers (*see the entire document, including Paragraphs 69-74*),

said timing sequence control unit (*wherein Paragraph 70 states: "the timing/gamma controller 142 [in FIGs. 14 & 15] is integrated into a single chip incorporating the gamma controller 91 and the memory 92 in FIG. 9"*) comprising:

a timing controller [*Fig. 9: 91*] receiving a system input [*Fig. 9: from 100*] and providing said clock signal [*Fig. 9: I^2C Clock*]; and

a color management control block [*Fig. 9: 91*], coupled to said timing controller, outputting said digital color management data and said clock signal to said plurality of source drivers [*Fig. 8: 83; Fig. 9: 96-99; Fig. 14: 143; Fig. 15: 154-156*],

said digital color management data is adjustable [*Fig. 9: via 100*] (*see the entire document, including Paragraphs 48-61 -- wherein the Gamma Modes A to D are selectable/adjustable via the user interface*).

Should it be shown that ***Kang*** discloses the claimed subject matter of "*gate/source drivers*" with insufficient specificity:

The ***AAPA*** discloses a color management structure [*Fig. 2*] for a panel display [*Fig. 2: 120*], comprising:

a display array unit [*Fig. 2: pixel array*];

a plurality of gate drivers [*Fig. 2: 124*];

a plurality of source drivers [*Fig. 2: 122*],

said plurality of gate drivers and said plurality of source drivers driving said display array unit to display an image; and

a timing sequence control unit [*Fig. 2: 126*],

said timing sequence control unit outputting a plurality of signals [*Fig. 2: clock & color data from 126 to 122 & 124*] to said plurality of gate drivers and said plurality of source drivers to drive said display array unit,

said timing sequence control unit outputting a clock signal [*Fig. 2: clock*] and

a digital color management data [*Fig. 2: color data*] to said plurality of source drivers (*see the entire **AAPA**, including Paragraphs 7-10*).

Kang and the ***AAPA*** are analogous art, because they are from the shared inventive field of driving, timing control, and gamma correction of liquid crystal displays.

Therefore, it would have been obvious to use the ***AAPA's*** gate/source drivers in the place of ***Kang's*** gate/source drivers, because the substitution of one known arrangement of gate/source drivers for another would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

See KSR International Co. v. Teleflex Inc., et al., Docket No. 04-1350 (U.S. 30 April 2007).

Regarding claim 2, ***Kang*** discloses said digital color management data is adjustable [*Fig. 9: via 100*] (*see the entire document, including Paragraphs 48-61 -- wherein the Gamma Modes A to D are selectable/adjustable via the user interface*).

Regarding claim 3, ***Kang*** discloses said panel display is a liquid crystal display (*see the entire document, including Paragraph 69*).

Regarding claim 6, ***Kang*** discloses each of said plurality of source drivers includes:

a source drive circuit [*Fig. 9: 97; Fig. 15: 156*] to drive said display array unit; and

a programmable data interface [*Fig. 9: 92, 93; Fig. 15: memory within 142, 152*] receiving said digital color management data [*Fig. 9: I^2C Data; Fig. 15: γ data*] and said clock signal [*Fig. 9: I^2C Clock; Fig. 15: Clock*] to parallel output a plurality of color voltage level

signals [*Figs. 9, 10: GMA*] to said source drive circuit (*see the entire document, including Paragraphs 48-61*).

Regarding claim 7, ***Kang*** discloses said plurality of color voltage level signals includes a plurality of color gamma voltage level data (*see the entire document, including Paragraphs 48-61 -- for red, green, and blue video data*).

Regarding claim 8, ***Kang*** discloses said programmable data interface includes:

an input interface [*Fig. 9: 92*] receiving said digital color management data [*Fig. 9: I^2C Data*] and said clock signal [*Fig. 9: I^2C Clock*] and translating said digital color management data [*Fig. 9: 6-bit serial gamma data*] via a data format;

a decoder [*Fig. 10: 101*] receiving said translated digital color management data and said clock signal and decoding said translated digital color management data, and outputting a decoded data [*Fig. 11: D5-D0*] and a control signal [*Fig. 11: A3-A0, SD-SA*]; and

a digital-to-analog converting unit [*Fig. 10: 103*] receiving said decoded data, said control signal, and said clock signal, and parallel outputting said plurality of color voltage level signals (*see the entire document, including Paragraphs 48-61 -- for red, green, and blue video data*).

The ***AAPA*** additionally discloses a digital-to-analog converting unit [*Fig. 1: 106*] receiving decoded data [*Fig. 1: VGMA1-VGMA14*], a control signal [*Fig. 1: POL*], and a clock

signal [*Fig. 1: CLK1*], and parallel outputting a plurality of color voltage level signals [*Fig. 1: Y1-Y384*] (*see the entire **AAPA**, including Paragraphs 7-10*).

Regarding claim 11, ***Kang*** discloses said timing sequence control unit is integrated into an application specified integrated circuit (*see the entire document, including Paragraph 70*).

The ***AAPA*** additionally discloses said timing sequence control unit is integrated into an application specified integrated circuit [*Fig. 2: ASIC*] (*see the entire **AAPA**, including Paragraphs 7-10*).

Response to Arguments

8. Applicant's arguments filed *20 July 2009* have been fully considered but they are not persuasive.

The Applicant contends, "*in **Kang**, the gamma controller 91 in Fig. 9 is not a constituent element of the timing/gamma controller 142 in Fig. 14. Please refer to **Kang** paragraph [0051], and **Kang** Figs. 8 and 9. Rather than being a constituent element of the timing/gamma controller 142 in Fig.14, the gamma controller 91 in Fig. 9 is in fact a constituent element of the multi-mode gamma voltage generator 84 in Fig. 8. According to Fig. 8, the multi-mode gamma voltage generator 84 and the controller 82 are two distinct elements that have no interaction. According to **Kang** paragraphs [0050] and [0071], the controller 82 in Fig. 8 is distinct from the timing/gamma controller 142 in Fig. 14. Therefore, unlike Applicant's currently amended claim*

*1, **Kang** fails to disclose that the timing sequence control unit comprises the timing controller and the color management control block*" (see Page 8 of the Response filed *20 July 2009*). However, the examiner respectfully disagrees.

Contrary to the Applicant's allegation that "*the gamma controller 91 in Fig. 9 is not a constituent element of the timing/gamma controller 142 in Fig. 14;*" ***Kang*** explicitly states, "*the timing/gamma controller 142 [in FIGs. 14 & 15] is integrated into a single chip incorporating the gamma controller 91 and the memory 92 in FIG. 9*" (see Paragraph 70).

Therefore, ***Kang*** does indeed disclose a timing sequence control unit [*Figs. 14 & 15: 142*] (*wherein Paragraph 70 states: "the timing/gamma controller 142 [in FIGs. 14 & 15] is integrated into a single chip incorporating the gamma controller 91 and the memory 92 in FIG. 9"*) comprising:

a timing controller [*Fig. 9: 91*] receiving a system input [*Fig. 9: from 100*] and providing said clock signal [*Fig. 9: I^2C Clock*]; and

a color management control block [*Fig. 9: 91*], coupled to said timing controller, outputting said digital color management data and said clock signal to said plurality of source drivers [*Fig. 8: 83; Fig. 9: 96-99; Fig. 14: 143; Fig. 15: 154-156*],

said digital color management data is adjustable [*Fig. 9: via 100*] (*see the entire document, including Paragraphs 48-61 -- wherein the Gamma Modes A to D are selectable/adjustable via the user interface*).

The Applicant contends, "*On page 7 of the final Office action, the Examiner states that the column driver 143 in Fig. 14 of* ***Kang*** *is equivalent to the source drivers of the original claim 1 of the present application. But this is the third embodiment of* ***Kang****, paragraph [0069], an LCD comprising a timing/gamma controller. Then on page 9 of the final Office action, the Examiner states that the gamma controller 91 in Fig. 9 of* ***Kang*** *is equivalent to the timing controller of the original claim 4 of the present application, but the gamma controller of Fig. 9 is from the first embodiment of* ***Kang****, paragraph [0048], which comprises a multi-mode gamma voltage generator.*

Currently amended claim 1 now includes claim 4, and so the timing controller of previously dependent claim 4 outputs (as it always has) to the same plurality of source drivers as claim 1. The examiner has the multi-mode gamma voltage generator from Fig. 9 serving as the timing/gamma controller from Fig. 14, but they are each from distinct embodiments, and not equivalent to Applicant's timing controller.

On page 7 of the final Office action, the Examiner first states that the clock in Fig.14 of ***Kang*** *is equivalent to the clock signal of the original claim 1 of the present application. Then, on page 9 of the final Office action, the Examiner contradictorily states that the* I^2C *clock in Fig.9 of* ***Kang*** *is equivalent to the clock signal of the original claims 1 and 4 of the present application. Because the* I^2C *clock in Fig.9 and the clock in Fig.14 are two distinct signals, they can not be equivalent to the clock signal of the original claims 1 and 4 of the present application at the same time.*

The I^2C *clock in Fig.9 of* ***Kang*** *is not provided to the column driver 143 in Fig.14, they are distinct and completely different embodiments, and the clock in Fig.14 is not provided by the*

gamma controller 91 in Fig.9. The gamma controller 91 in Fig.9 does not provide any signal for the column driver 143 in Fig.14. Therefore, unlike the currently amended claim 1, ***Kang*** *fails to disclose that the timing controller provides the clock signal for the source drivers.*

On page 7 of the final Office action, the Examiner states that the column driver 143 in Fig.14 of ***Kang*** *is equivalent to the source drivers of the original claim 1 of the present application. But again the gamma controller 91 in Fig.9 does not output any signal to the column driver 143 in Fig.14. In addition, the I^2C clock in Fig.9 is not output to the column driver 143 in Fig.14. Therefore, unlike the currently amended claim 1,* ***Kang*** *fails to disclose that the timing controller provides the clock signal for the source drivers*" (see Pages 8-10 of the Response filed *20 July 2009*). However, the examiner respectfully disagrees.

Contrary to the Applicant's allegation that the gamma controller 91 in Fig. 9 is from an embodiment entirely distinct from the timing/gamma controller 142 in Fig. 14; ***Kang*** explicitly states, "*the timing/gamma controller 142 [in FIGs. 14 & 15] is integrated into a single chip incorporating the gamma controller 91 and the memory 92 in FIG. 9*" (see Paragraph 70).

Therefore, ***Kang*** does indeed disclose a timing sequence control unit [*Figs. 14 & 15: 142*] (*wherein Paragraph 70 states: "the timing/gamma controller 142 [in FIGs. 14 & 15] is integrated into a single chip incorporating the gamma controller 91 and the memory 92 in FIG. 9"*) comprising:

a timing controller [*Fig. 9: 91*] receiving a system input [*Fig. 9: from 100*] and providing said clock signal [*Fig. 9: I^2C Clock*]; and

a color management control block [*Fig. 9: 91*], coupled to said timing controller, outputting said digital color management data and said clock signal to said plurality of source drivers [*Fig. 8: 83; Fig. 9: 96-99; Fig. 14: 143; Fig. 15: 154-156*],

said digital color management data is adjustable [*Fig. 9: via 100*] (*see the entire document, including Paragraphs 48-61 -- wherein the Gamma Modes A to D are selectable/adjustable via the user interface*).

The Applicant contends, "***Kang*** *also fails to disclose that the color management control block outputs the digital color management data and the clock signal to the source drivers.*

On page 9 of the final Office action, the Examiner states that the gamma controller 91 in Fig.9 of ***Kang*** *is equivalent to the color management control block of the original claim 4 of the present application. Previously, on page 7 of the final Office action, the Examiner stated that either the γ data in Fig.14 or the I^2C data in Fig.9 of* ***Kang*** *is equivalent to the digital color management data of the original claim 1 of the present application, but because the I^2C data in Fig.9 and the γ data in Fig.14 are two distinct signals, they cannot be equivalent to the digital color management data of the original claim 1 of the present application at the same time. Neither is the clock in Fig. 14 output by the gamma controller 91 in Fig.9, nor is the γ data in Fig.14 output by the gamma controller 91 in Fig.9*" (see Page 10 of the Response filed *20 July 2009*). However, the examiner respectfully disagrees.

Contrary to the Applicant's allegation that the gamma controller 91 in Fig. 9 is from an embodiment entirely distinct from the timing/gamma controller 142 in Fig. 14; ***Kang*** explicitly

states, "*the timing/gamma controller 142 [in FIGs. 14 & 15] is integrated into a single chip incorporating the gamma controller 91 and the memory 92 in FIG. 9*" (see Paragraph 70).

Therefore, ***Kang*** does indeed disclose a timing sequence control unit [*Figs. 14 & 15: 142*] (*wherein Paragraph 70 states: "the timing/gamma controller 142 [in FIGs. 14 & 15] is integrated into a single chip incorporating the gamma controller 91 and the memory 92 in FIG. 9"*) comprising:

a timing controller [*Fig. 9: 91*] receiving a system input [*Fig. 9: from 100*] and providing said clock signal [*Fig. 9: I^2C Clock*]; and

a color management control block [*Fig. 9: 91*], coupled to said timing controller, outputting said digital color management data and said clock signal to said plurality of source drivers [*Fig. 8: 83; Fig. 9: 96-99; Fig. 14: 143; Fig. 15: 154-156*],

said digital color management data is adjustable [*Fig. 9: via 100*] (*see the entire document, including Paragraphs 48-61 -- wherein the Gamma Modes A to D are selectable/adjustable via the user interface*).

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571)272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
25 September 2009